**CLAIMS**

What is claimed is:

1. A method comprising, comprising:

    a) driving a first current through a line and a termination resistance so that a logical value on said line changes from a first logical value to a second logical value; and

    b) holding said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current.

2. The method of claim 1 wherein said first and second currents flow in a direction from said line into said termination resistance.

3. The method of claim 2 wherein said second logical value is a logical high.

4. The method of claim 2 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

5. The method of claim 1 wherein said first and second currents flow in a direction from said termination resistance into said line.

6. The method of claim 5 wherein said second logical value is a logical low.

7. The method of claim 5 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

8. The method of claim 1 wherein said first current is sustained for less than a width of a bit that is propagated on said line.

9. The method of claim 1 wherein said first current is sustained for a width of a bit that is propagated on said line.

10. The method of claim 1 wherein said driving a first current further comprises applying a first multiplexer select line state to a multiplexer so that a first word is provided at an output of said multiplexer, said first word enabling a first number of sub-drivers, and said driving a second current further comprises applying a second multiplexer select line state to said multiplexer so that a second word is provided at said output of said multiplexer, said second word enabling a second number of said sub-drivers, said first number greater than said second number.

11. A method comprising, comprising:

a) driving a first current through a line and a termination resistance so that a logical value on said line changes from a first logical value to a second logical value, said first current sustained for a width of a first bit that is propagated on said line; and

b) holding said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current, said second current sustained for a width of a second bit that is propagated on said line.

12. The method of claim 11 wherein said first and second currents flow in a direction from said line into said termination resistance.

13. The method of claim 12 wherein said second logical value is a logical high.

14. The method of claim 12 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

15. The method of claim 11 wherein said first and second currents flow in a direction from said termination resistance into said line.

16. The method of claim 15 wherein said second logical value is a logical low.

17. The method of claim 15 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

18. The method of claim 11 wherein said first bit width is coextensive with a clock cycle.

19. The method of claim 11 wherein said driving a first current further comprises applying a first multiplexer select line state to a multiplexer so that a first word is provided at an output of said multiplexer, said first word enabling a first number of sub-drivers, and said driving a second current further comprises applying a second multiplexer select line state to said multiplexer so that a second word is provided at said output of said multiplexer, said second word enabling a second number of said sub-drivers, said first number greater than said second number..

20. An apparatus, comprising:

a driver that drives a first current through a line and a termination resistance so that a logical value on said line changes from a first .

logical value to a second logical value, wherein said driver holds said second logical value on said line by driving a second current through said line and said termination resistance, said second current less than said first current.

21. The apparatus of claim 20 wherein said first and second currents flow in a direction from said line into said termination resistance.

22. The apparatus of claim 21 wherein said second logical value is a logical high.

23. The apparatus of claim 21 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said line by said second current.

24. The apparatus of claim 20 wherein said first and second currents flow in a direction from said termination resistance into said line.

25. The apparatus of claim 24 wherein said second logical value is a logical low.

26. The apparatus of claim 24 wherein said first current produces a first voltage on said line that is smaller than a second voltage produced on said line by said second current.

27. The apparatus of claim 20 wherein said first current is sustained for less than a width of a bit that is propagated on said line.

28. The apparatus of claim 20 wherein said first current is sustained for a width of a bit that is propagated on said line.

29. The apparatus of claim 20 further comprising a multiplexer that provides a first word that enables a first number of sub-drivers, and provides a second word that enables a second number of said sub-drivers drivers, said first number greater than said second number.

30. An apparatus, comprising:

a driver that drives a first current through an address line and a termination resistance so that a logical value on said address line changes from a first logical value to a second logical value, wherein said driver holds said second logical value on said address line by driving a second current through said address line and said termination resistance, said second current less than said first

current, said address line coupled to a memory device that receives said logical value.

31. The apparatus of claim 30 wherein said first and second currents flow in a direction from said address line into said termination resistance.

32. The apparatus of claim 30 wherein said second logical value is a logical high.

33. The apparatus of claim 30 wherein said first current produces a first voltage on said line that is larger than a second voltage produced on said address line by said second current.

34. The apparatus of claim 30 wherein said first and second currents flow in a direction from said termination resistance into said address line.

35. The apparatus of claim 34 wherein said second logical value is a logical low.

36. The apparatus of claim 34 wherein said first current produces a first voltage on said address line that is smaller than a second voltage produced on said address line by said second current.

37. The apparatus of claim 30 wherein said first current is sustained for less than a width of a bit that is propagated on said line.

38. The apparatus of claim 30 wherein said first current is sustained for a width of a bit that is propagated on said line.

39. The apparatus of claim 30 further comprising a multiplexer that provides a first word that enables a first number of sub-drivers, and provides a second word that enables a second number of said sub-drivers drivers, said first number greater than said second number..